ABSTRACT

A process and a package for achieving wafer scale packaging is described. A layer of a polymeric material, such as polyimide, silicone elastomer, or benzocyclobutene is deposited on the surface of a chip. Via holes through this layer connect to the top surfaces of the studs that pass through the passivating layer of the chip. In one embodiment, the polymeric layer covers a redistribution network on a previously planarized surface of the chip. Individual chip-level networks are connected together in the kerf so that conductive posts may be formed inside the via holes through electroplating. After the formation of solder bumps, the wafer is diced into individual chips thereby isolating the individual redistribution networks. In a second embodiment, no redistribution network is present so electroless plating is used to form the posts. In a third embodiment, there is also no redistribution network but electroplating is made possible by using a contacting layer. Solder bumps attached to the posts are then formed by means of electroless plating, screen or stencil printing.